REMARKS

Claims 8-14 are pending.

At page 2 of the Action, Claim 13 has been objected to as allegedly being in improper form because "a multiple dependent claim cannot be dependent upon other dependent claims."

With due respect, the Examiner's position is not reasonable.

A multiple dependent claim is a dependent claim which refers back in the alternative to more than one preceding independent or *dependent* claim. A multiple dependent claim cannot depend from another multiple dependent claim. See, MPEP § 608.01(n).

Present Claim 13 recites "[t]he method according to any one of claims 8 to 12, ..." Claim 8 is an independent claim. Claims 9-12 each depend only on Claim 8.

Accordingly, present Claim 13 is a proper multiple dependent claim. Withdrawal of the objection to Claim 13 is requested.

At page 3 of the Action, Claims 8-13 have been rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Fitzgerald (US 2002/0052061) in view of JP 52-106380 (Abstract, "JP '380").

At page 4 of the Action, Claim 14 has been rejected under 35 U.S.C. § 103(a) as being unpatentable over Fitzgerald in view of JP '380, and further in view of Waldrop et al (US 4,999,685).

Applicant submits that the above two rejections should be withdrawn because Fitzgerald, JP '380 and Waldrop et al do not disclose or render obvious the present invention, either alone or in combination.

Independent Claims 8 and 14 recite that "said steps are performed in a same epitaxial growth furnace." That is, the present invention requires conducting the epitaxial growth of a

III-V group compound semiconductor single crystal and the epitaxial growth for forming a Si layer in a same epitaxial growth furnace. This feature clearly distinguishes the present invention from the cited references.

In the Response under 37 C.F.R. § 1.111 filed April 24, 2009, Applicant explained that JP '380 does not teach the growth of the III-V group compound semiconductor layer and the IV group semiconductor layer (Si layer) in the same epitaxial growth furnace. In other words, JP '380 only discloses the sequential growth of a plurality of III-V group compound semiconductor layers in the same epitaxial growth furnace. Thus, JP '380 does not make for the deficiencies of Fitzgerald.

Applicant further explained that Fitzgerald and JP '380 do not teach or suggest the superior results provided by the present invention, that is, the presently claimed method for producing a thin film crystal wafer for a III-V group compound semiconductor device provides a thin film crystal wafer excellent in ohmic property.

In response, the Examiner considers that Applicant was arguing apparatus limitations in process claims.

The Examiner then contends that apparatus limitations may have little weight in process claims and that it has been held that to be entitled to weight in method claims, the recited structure limitations therein must affect the method in a manipulative sense, and not to amount to the mere claiming of a use of a particular structure.

However, the limitation that "said steps are performed in a same epitaxial growth furnace" is not an apparatus limitation; rather, it is a process limitation.

Accordingly, the Examiner is respectfully requested to reconsider her position.

Further, when a semiconductor is formed, a very small amount of impurities often causes significant problems. In the technical field relating to the present invention, the III-V group compound can become an impurity for Si. Based on this common knowledge, a person skilled in the art would have been concerned that the presence of the III-V group compound would adversely affect the products as an impurity. Accordingly, a person skilled in the art would not have conceived of sequentially conducting the growth of the III-V group compound semiconductor layer and the IV group semiconductor layer in the same growth furnace.

However, the present inventor has accomplished the present invention by sequentially conducting the growth of the III-V group compound semiconductor layer and the IV group semiconductor layer in the same furnace, and the present invention provides excellent ohmic electrode which the cited references do not teach or suggest.

Accordingly, the present claims are not obvious and are patentable over Fitzgerald and JP '380, either alone or in combination.

Waldrop et al is relied upon as teaching depositing a metal-to-semiconductor contact, such as Au, Cr or Ti, on a heavily doped p-type layer of silicon. The interface layer is deposited on gallium arsenide (abstract). Waldrop et al does not make up for the deficiencies of Fitzgerald and JP '380.

In view of the above, reconsideration and withdrawal of the §103(a) rejections based on Fitzgerald, JP '380 and Waldrop et al are respectfully requested.

Allowance is respectfully requested. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,

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Date: October 21, 2009